

3.9. Exercises

EXERCISE 3.1.– Implementation of logic gates using 2 : 1 multiplexer.

Show that the circuits in Figure 3.60(a)–3.60(d) are equivalent to the AND, OR, XOR and NAND logic gates, respectively.

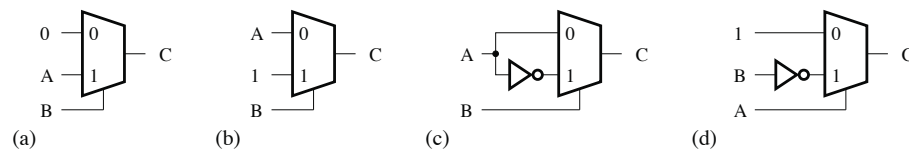


Figure 3.60. Logic circuits with multiplexers

EXERCISE 3.2.– Implementation of 2-out-of-4 decoder using 1-to-2 multiplexers.

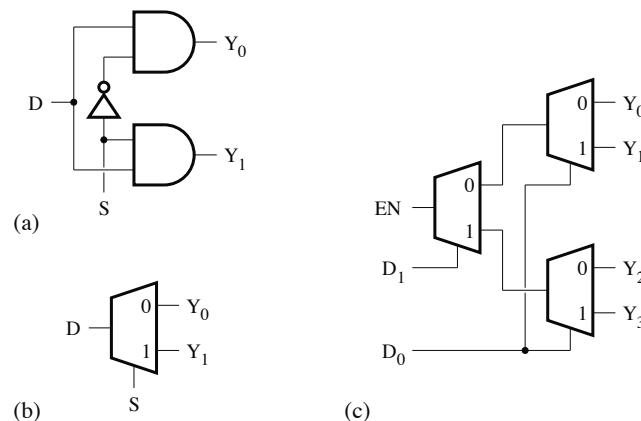


Figure 3.61. 2 : 4 decoder based on 1-to-2 multiplexers

1) Verify that the logic circuit shown in Figure 3.61(a) implements a 1-to-2 demultiplexer, whose symbol is given in Figure 3.61(b).

2) To determine the function of the logic circuit illustrated in Figure 3.61(c), find the logic equations for the outputs and draw up the truth table.

EXERCISE 3.3.– Realization of 2-to-4 decoder using NAND gates.

To determine the role of the logic circuit shown in Figure 3.62, find the logic equations for the outputs and draw up the corresponding truth table.

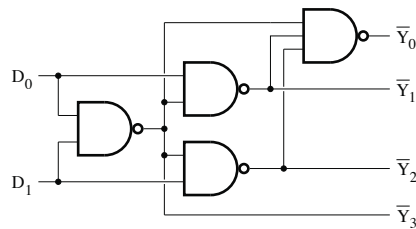


Figure 3.62. 2-out-of-4 encoder with NAND gates

EXERCISE 3.4.– 8 : 3 priority encoder.

To determine the role of the logic circuit shown in Figure 3.63, find the logic equations for the outputs and draw up the corresponding truth table.

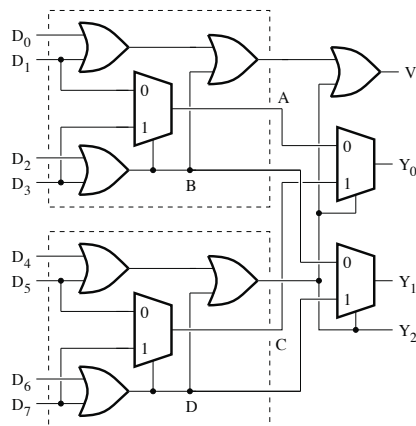


Figure 3.63. 8:3 priority encoder

EXERCISE 3.5.– Implementation of the function $F(A, B, C)$.

Implement the logic function $F(A, B, C)$, which is characterized by the truth table shown in Table 3.33 using a 2 : 1 multiplexer and logic gates to be determined.

EXERCISE 3.6.– 4-to-1 multiplexer.

Determine the logic equation for the output and construct the truth table for the multiplexer shown in Figure 3.64.

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Table 3.33. Truth table of the function $F(A, B, C)$

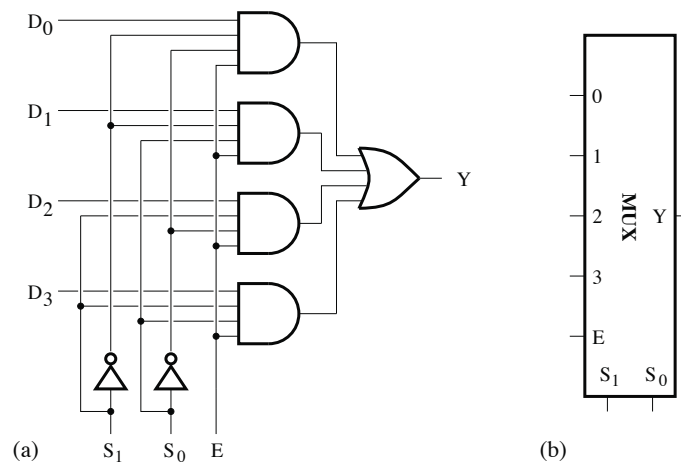


Figure 3.64. a) 4-to-1 multiplexer with enable signal; b) symbol

Use a 4-to-1 multiplexer and logic gates to implement the function:

$$F(A, B, C, D) = \sum m(3, 4, 5, 6, 7, 9, 10, 12, 14, 15) \quad [3.75]$$

EXERCISE 3.7.– Demultiplexer/decoder.

Draw up the truth table for the decoder in Figure 3.65(a).

What is the difference between a decoder and demultiplexer?

Analyze the logic circuit shown in Figure 3.65(b) and determine the logic equations for the outputs $Z_i(A, B, C, D)$ with $i = 0, 1, 2, 3$.

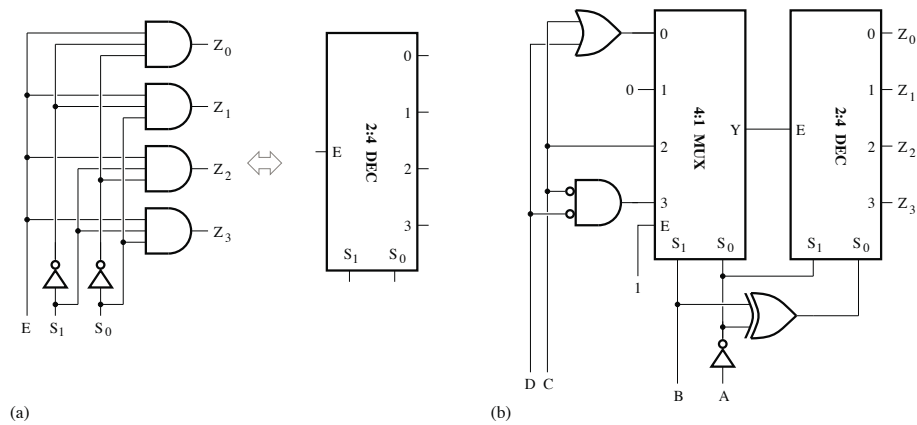


Figure 3.65. a) 2 : 4 decoder with an enable input; b) logic circuit

EXERCISE 3.8.– Implementation of the function $F(A, B, C, D)$.

Implement the function, $F(A, B, C, D)$, whose logic expression is written as:

$$F(A, B, C, D) = A \oplus B \oplus C \oplus D \quad [3.76]$$

using a 4 : 1 multiplexer and logic gates to be determined.

EXERCISE 3.9.– Majority function of three variables.

The majority function, F , of three variables takes either the logic level 1, if the majority (two or three) of the variables is at logic level 1, or the logic level 0 in all other cases:

- construct the truth table of the function F ;
- determine and simplify the logic equation for the function F ;
- implement the function F using a 4 : 1 multiplexer.

EXERCISE 3.10.– 8-to-1 multiplexer.

Verify by determining the logic equation for the output and by constructing the truth table when each of the logic circuits shown in Figure 3.66 works as an 8-to-1 multiplexer.

Use an 8-to-1 multiplexer and logic gates to implement the following function:

$$F(A, B, C, D, E) = \sum m(0, 1, 2, 4, 5, 6, 7, 13, 14, 20, 21, 22, 28, 29, 30, 31) \quad [3.77]$$

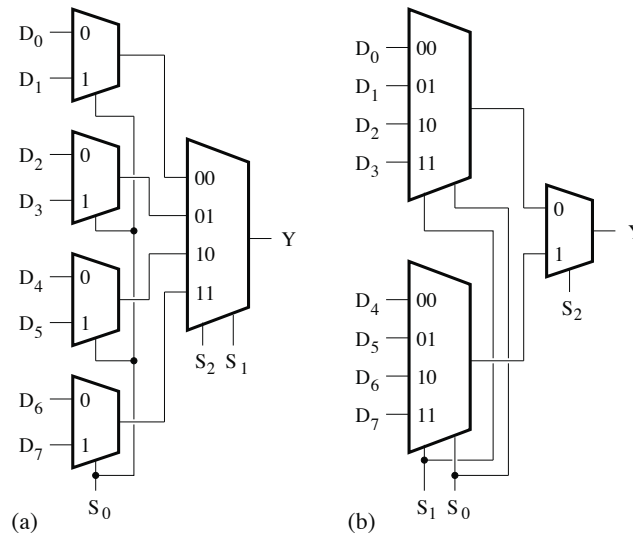


Figure 3.66. Implementation of an 8-to-1 multiplexer based on a) four 2-to-1 multiplexers or b) two 4-to-1 multiplexers

EXERCISE 3.11.– Implementation of a logic function based on a decoder

Implement the logic function:

$$F(A, B, C, D) = \sum m(1, 3, 7, 9, 15) \quad [3.78]$$

using a 3 : 8 decoder with enable input $\overline{EN}$, a 5-input NAND gate and 2-input NAND gates. The decoder has active-low outputs.

EXERCISE 3.12.– Analysis of a logic circuit.

Determine the logic equation for each of the outputs Y_i ($i = 0, 1, 2, \dots, 7$) of the logic circuit shown in Figure 3.67.

Draw up the truth table for this circuit.

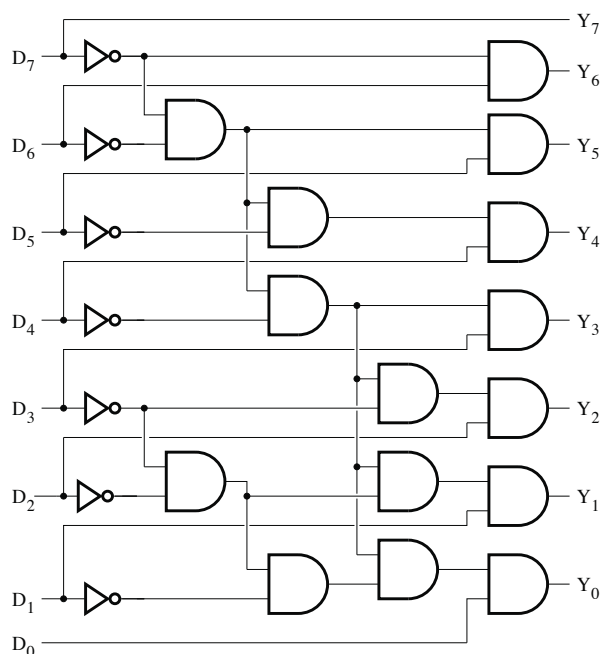


Figure 3.67. Logic circuit

What is the role of this circuit?

EXERCISE 3.13.– Design of a multiplier for 2-bit binary words.

We wish to implement a multiplier according to the following specifications:

- inputs: $X = X_1X_0$ and $Y = Y_1Y_0$;
- output: $Z = X \cdot Y$ where $Z = Z_3Z_2Z_1Z_0$.

Construct the truth table for this multiplier.

Determine the Boolean expressions for each of the outputs Z_i ($i = 0, 1, 2, 3$).

Implement this multiplier using logic gates.

EXERCISE 3.14.– Comparator for 2-bit binary numbers.

Implement a comparator for 2-bit numbers: $P = AB$ and $Q = CD$ (see Figure 3.68).

Draw up the truth table for this comparator.

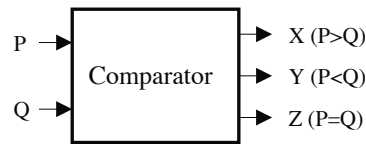


Figure 3.68. *Comparator*

Deduce and simplify the logic expressions for X, Y and Z.

Propose a logic circuit for the implementation of this comparator.

EXERCISE 3.15.– BCD-to-7-segment decoder.

A 4-bit number, A, B, C, D (D is the LSB), is applied to the inputs of the decoder supplying the signals a, b, c, d, e, f and g that are used to drive a 7-segment display (see Figure 3.69) generating numbers from 0 to 9.

Draw up the truth table for this decoder.

Deduce and simplify the logic expressions for a, b, c, d, e, f and g.

Propose a logic circuit that can be used to realize the decoder.

We will assume that the diodes of the display are controlled by low-level signals.

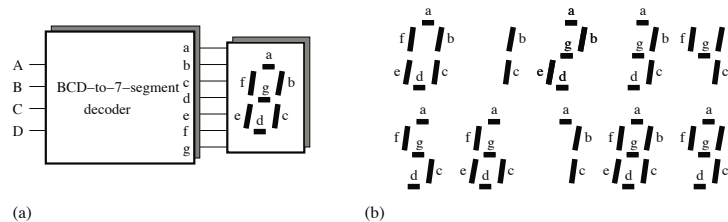


Figure 3.69. *a) BCD-to-7-segment decoder;
b) display of numbers from 0 to 9*

EXERCISE 3.16.– HEX-to-7-segment decoder.

A number consisting of 4 bits, A, B, C and D (D is the LSB), is applied to the inputs of the decoder supplying the signals a, b, c, d, e, f and g that are used to drive a 7-segment display (see Figure 3.70) generating the numbers from 0 to 9 and the letters A–F corresponding to the hexadecimal representation of the numbers 10–15.

Draw up the truth table for the decoder, assuming that the diodes of the display are controlled by low-level signals.

Deduce and simplify the logic expressions for $\bar{a}$, $\bar{b}$, $\bar{c}$, $\bar{d}$, $\bar{e}$, $\bar{f}$ and $\bar{g}$.

Propose a logic circuit that can be used to implement the decoder, using logic gates with no more than four inputs.

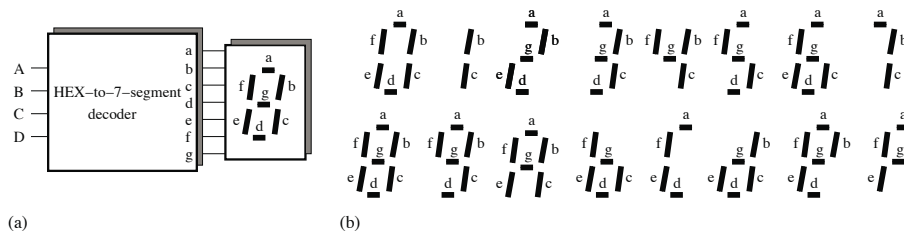


Figure 3.70. a) HEX-to-7-segment decoder; b) display of numbers from 0 to 9 and letters A–F

EXERCISE 3.17.– Analysis of logic circuits:

– analyze the logic circuit shown in Figure 3.71 and determine its function. The inputs are represented by X_4, X_3, X_2, X_1, X_0 and X_{-1} ; the outputs by Y_3, Y_2, Y_1 and Y_0 ; and the control signals by D, S and E ;

– same question for the logic circuit based on 2 : 1 multiplexers and which is represented in Figure 3.72, where the data inputs are denoted by $D_7, D_6, D_5, D_4, D_3, D_2, D_1$ and D_0 ; the outputs by $Y_7, Y_6, Y_5, Y_4, Y_3, Y_2, Y_1$ and Y_0 ; and the control signals by S_2, S_1 and S_0 .

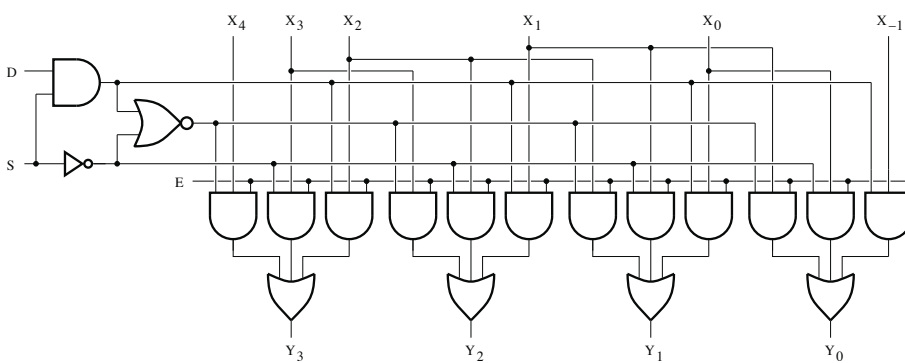


Figure 3.71. Logic circuit 1